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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/750,111	12/29/2000	Wendell P. Noble JR.	M4065.0019/P019-A	6297

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EXAMINER
ROSE, KIESHA L

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 02/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/750,111	Applicant(s) NOBLE ET AL.	
	Examiner Kiesha L. Rose	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to the election filed 2 December 2002.

Election/Restrictions

Claims 47-54 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected method of making a semiconductor device, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 5 and 8.

Applicant's election without traverse of Claims 1-33 in Paper No. 5 and 8 is acknowledged.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitagawa (U.S. Patent 5,329,142) in view of Agnello (U.S. Patent 5,776,823).

Kitagawa discloses a semiconductor device (Figs. 2,6,7 and 27) that contains a substrate (12) for supporting gated lateral complementary vertical bipolar transistors

that are p-n-p and n-p-n transistors (Q) where the collector region of the p-n-p is connected to the base region of the n-p-n.

In regards to claim 14, the vertical transistor is formed in a trench within the substrate

Kitagawa discloses all of the limitations except for the p-type gate to be connected to the n-region and the n-type gate to be connected to the p-region. Whereas Agnello discloses a SRAM that contains a p-type gate connected to the n-region and the n-type gate connected to the p-region. The gate connection is formed to have optimal work function. (Fig. 5, col. 2, lines 1-8) Since Kitagawa and Agnello are both from the same field of endeavor, semiconductor devices, the purpose disclosed by Agnello would have been recognized in the pertinent art of Kitagawa. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kitagawa by incorporating the p-type gate to be connected to the n-region and the n-type gate to be connected to the p-region to have optimum work function as taught by Agnello.

In regards to claims 6-7 and 12, they disclose the gates to have a certain bias by pulse gate bias, it would have been obvious to one having ordinary skill in the art at the time the invention was made to bias the gates of the transistors to supply current to the device as a matter of design choice.

In regards to claims 9 and 16, Kitagawa and Agnello disclose the claimed invention except the memory cell to have an area of about $4F^2$. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the

memory cell to have an area of about $4F^2$, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (1980).

Claims 17-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitagawa and Agnello.

Kitagawa discloses a semiconductor device (Figs. 2,6,7,21 and 27) that contains a substrate (12) for supporting a gated lateral complementary vertical bipolar transistors that are p-n-p and n-p-n transistors (Q) where the gates are connected to the p- channel region of the transistor in the trenches, the first trenches are between the transistors and the second trenches are orthogonal to the first trenches, an oxide insulating layer (2100) between the transistor and the substrate 305, horizontally isolating the transistors in the n- region. Kitagawa discloses all of the limitations except the p-type gate to be connected to the n-region and the n-type gate to be connected to the p-region. Whereas Agnello discloses a SRAM (Fig. 5) that contains p-type gates to be connected to the n-region and the n-type gates to be connected to the p-region for optimum work function. (Col. 2, lines 1-8) Since Kitagawa and Agnello are both from the same field of endeavor, memory devices, the purpose disclosed by Agnello would have been recognized in the pertinent art of Kitagawa. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kitagawa by incorporating p-type gates to be connected to the n-region and the n-type gates to be connected to the p-region for optimum work function as taught by Agnello.

In regards to claims 17-19, dealing with the gates connected to at least one voltage source and providing a pulse gate bias, it would have been obvious to one having ordinary skill in the art at the time the invention was made to connect the gates to at least one voltage source and provide a pulse gate bias as a matter of design choice to supply current to the device.

Claims 28-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitagawa and Agnello in view of Kurth et al. (U.S. Publication 2001/0021122).

Kitagawa discloses a semiconductor device (Figs. 2,6,7 and 27) that contains a substrate (12) for supporting a gated lateral complementary vertical bipolar transistors that are p-n-p and n-p-n transistors (Q) where the collector region of the p-n-p is connected to the base region of the n-p-n. Kitagawa discloses all of the limitations except for the p-type gate to be connected to the n-region and the n-type gate to be connected to the p-region. Whereas Agnello discloses a SRAM that contains a p-type gate connected to the n-region and the n-type gate connected to the p-region. The gate connection is formed to have optimal work function. (Fig. 5, col. 2, lines 1-8) Since Kitagawa and Agnello are both from the same field of endeavor, semiconductor devices, the purpose disclosed by Agnello would have been recognized in the pertinent art of Kitagawa. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kitagawa by incorporating the p-type gate to be connected to the n-region and the n-type gate to be connected to the p-region to have optimum work function as taught by Agnello.

In regards to claims 30-31, they disclose the gates to have a certain bias by pulse gate bias, it would have been obvious to one having ordinary skill in the art at the time the invention was made to bias the gates of the transistors to supply current to the device as a matter of design choice.

In regards to claim 33, Kitagawa and Agnello disclose the claimed invention except the memory cell to have an area of about $4F^2$. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the memory cell to have an area of about $4F^2$, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (1980).

Kitagawa and Agnello disclose all of the limitations except having a computer system. Whereas Kurth discloses a memory cell (Fig. 19) that contains a computer system with a processor (302) and a memory circuit (304). A computer system is added to process the stored information in the memory device. (Page 4, Paragraph 54) Since Kitagawa, Agnello and Kurth are both from the same field of endeavor, memory devices, the purpose disclosed by Kurth would have been recognized in the pertinent art of Kitagawa and Agnello. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the devices of Kitagawa and Agnello by incorporating a computer system to process the stored information in the memory cells as taught by Kurth.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 703-605-4212. The examiner can normally be reached on M-F 8:30-6:00 off 1st Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

KLR
February 24, 2003

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800